AJEENKYA
D Y PATIL UNIVERSITY

End Term Examination (December 2019)

School: School of Engineering **Program: BTECH (MACT/CTIS)**

Course: Computer Architecture & Its Organization **Course Code: CSC221**

Semester: 3 **Max Marks: 30** **Duration (mins) :** 60 Min

Note- 1. Figures to the right indicates full marks
2. Attempt any three questions.

Q1) a)Multiply 13 & -6 using Booth's Algorithm. (5)

b) Explain logical & arithmetic shift operations with examples. (5)

Q2) a) What is locality of reference property of cache memory? (2)

b) Briefly describe 3 phases of instruction cycle. (8)

Q3) a) Using register transfer notation show data transfer from R1 to R2. (2)

b)If reg.R has 0100 what would be R'(complement) ? (2)

c)Explain register direct and register indirect addressing modes. (6)

Q4) c) How stack is used to handle different function calls? Explain with figure. (5)

d) What page replacement techniques are used for virtual memory? (5)

Q5) a) Name different instruction formats. (2)

b) Explain Direct Memory Access in detail. (8)

*******ALL THE BEST*******